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PHOTOELECTRIC CONVERTER AND ITS MANUFACTURING METHOD
[KODENHENKANSOCHI OYOBI SONO SEIZOHOHO]

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[Claims] /*

[Claim 1] A photoelectric converter having photodiodes formed on a respective light-receiving region on the first conductivity-type semiconductor substrate, and

semiconductor circuit elements formed in regions other than said light-receiving regions on said semiconductor substrate;

further having an element-isolating structure formed on said semiconductor substrate, which has insulating film buried in a concave section, for isolating elements between said photodiodes and said semiconductor circuit elements; a second conductivity-type channel stopper layer formed in said semiconductor substrate which contacts and surrounds said element-isolating structure for isolating said photodiodes;

a first conductivity-type semiconductor layer, formed on the front side of said light-receiving region, that constitutes said photodiode;

a second conductivity-type first well, formed at the outside position of said light-receiving region against the edge of said element-isolating structure on said light-receiving region side, so as to surround said light-receiving region;

a second conductivity-type second well formed at the bottom section of said light-receiving region; and

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* Claim and paragraph numbers correspond to those in the foreign text.

a second conductivity-type third well which connects said first and second wells;

wherein

said channel stopper layer terminates at a specific position in said first well contacting with and surrounding said element-isolating structure and between the peripheral area of said light-receiving region and said semiconductor circuit element.

[Claim 2] The photoelectric converter according to Claim 1, wherein said element-isolating structure is provided at least at the peripheral of said light-receiving region.

[Claim 3] The photoelectric converter according to Claim 2, wherein said element-isolating structure is provided between said photodiode in said light-receiving region and said semiconductor circuit element in surrounding non-light-receiving section, and/or between said semiconductor circuit element in said non-light-receiving section and said semiconductor element in the surrounding circuit section.

[Claim 4] The electromagnetic converter according to Claim 3, wherein said first well is also formed in regions of said semiconductor circuit element of said non-light-receiving section and/or said semiconductor circuit element of said peripheral circuit section, and a channel stopper layer of lower density than the previously mentioned channel stopper layer is also formed in said

first well adjacent to said element-isolating structure around said semiconductor circuit element.

[Claim 5] The photoelectric converter according to Claim 1, wherein said element-isolating structure is an STI (Shallow Trench Isolation) structure.

[Claim 6] The photoelectric converter according to Claim 1, wherein said photoelectric converter is a solid-state photographing device.

[Claim 7] Manufacturing method of a photoelectric converter, which forms photodiodes on the respective light-receiving region on the first conductivity-type semiconductor substrate, and forms semiconductor circuit elements in regions other than said light-receiving regions on said semiconductor substrate; having a process that forms a concave section for isolating said photo diode and said semiconductor circuit element, and forms an element-isolating structure by burying insulating film in this concave section; a process that forms a second conductivity-type channel stopper layer, in said semiconductor substrate which contacts and surrounds said element-isolating structure, for isolating said photodiodes; a process for forming a first conductivity-type semiconductor layer on the front side of said light-receiving region that constitutes said photodiode; a process to form a second conductivity-type first well, at outside position of said light-receiving region against the edge of said element-isolating structure on said light-receiving region

side, so as to surround said light-receiving region; a process to form a second conductivity type second well at the bottom section of said light-receiving region; and a process to form a second conductivity-type third well which connects said first and second wells; wherein said channel stopper layer terminates at a specific position in said first well contacting with and surrounding said element-isolating structure and between the peripheral area of said light-receiving region and said semiconductor circuit element.

[Claim 8] The photoelectric converter according to Claim 7, wherein said element-isolating structure is provided at least at the peripheral of said light-receiving region.

[Claim 9] The photoelectric converter according to Claim 8, wherein said element-isolating structure is provided between said photodiode in said light-receiving region and said semiconductor circuit element in surrounding non-light-receiving section, and/or between said semiconductor circuit element in said non-light-receiving section and said semiconductor element in the surrounding circuit section.

[Claim 10] The manufacturing method of a electromagnetic converter according to Claim 9, wherein said first well is also formed in regions of said semiconductor circuit element of said non-light-receiving section and/or said semiconductor circuit element of said peripheral circuit section, and a channel stopper layer of lower density than the previously mentioned channel stopper layer is also

formed in said first well adjacent to said element-isolating structure around said semiconductor circuit element.

[Claim 11] The manufacturing method of a photoelectric converter according to Claim 7, wherein said element-isolating structure is an STI (Shallow Trench Isolation) structure.

[Claim 12] The manufacturing method of a photoelectric converter according to Claim 7, wherein, after said concave section is formed and prior to burying said insulating film in said concave section, said channel stopper layer is formed by injecting ion from the wall surface of said concave section of photodiode section while masking the peripheral area of a photodiode other than said photodiode section.

[Claim 13] The manufacturing method of a photoelectric converter according to Claim 10, wherein, after said concave section is formed and prior to burying said insulating film in said concave section, said channel stopper layer of said semiconductor circuit element section is formed by injecting ion from the wall surface of said concave section of the photodiode section while masking the photodiode section and semiconductor circuit element section of said non-light-receiving section and/or semiconductor circuit element section of said peripheral circuit section.

[Claim 14] The manufacturing method of a photoelectric converter according to Claim 7, wherein, after forming said concave section,

insulating material for element isolation is buried in said concave section by a vapor growth method.

[Claim 15] The manufacturing method of a photoelectric converter according to Claim 7, wherein said first, second, and third wells are formed by an ion injection method.

[Claim 16] The photoelectric converter according to Claim 7, which manufactures the solid-state photographing device.

[Detailed Description of the Invention]

[0001] [Technical Field of the Invention]

This invention is related to a photoelectric converter having photodiodes in each light-receiving region and to its manufacturing method.

[0002] [Prior Art]

In recent years, with rapid and widespread use of digital cameras and the Internet, there are increasing occasions when optical image information is converted into electric signals as digital data and are processed and utilized. For this reason, there in an increasing demand for photoelectric converters such as solid-state photographing devices, etc, to have higher performance in the form of smaller size, lower cost, higher resolution, higher sensitivity, and wider dynamic range, etc. Consequently, it is expected that solid-state photographing elements such as photodiodes would be further miniaturized and have a higher degree of integration.

[0003] Figure 9 is an example of a skeleton cross-sectional view (a) and a skeleton top view (b) of major parts of a photo diode (PD: Photo Diode) of a conventional image sensor, etc. An element-isolating structure 107 with a LOCOS (Local Oxidation of Silicon) structure, for electrically insulating light-receiving region 114 of each photodiode and for a isolating photodiode from each other, is formed on the surface of the substrate.

[0004] In the example shown in Figure 9, n-type silicon substrate 101 is used for the substrate, and a photodiode is formed by pn-bonding of n-type silicon layer 118 formed on the substrate surface and the silicon layer 112 converted to p^--type below it at their boundary. Hereafter, the section surrounded by element-isolating structure 107 is called a light-receiving region 114, and its section with a pn-joint is called a sensor opening section 115, for distinction.

[0005] Light entering the sensor opening section 115 is converted into an electron hole and electron when it reaches the pn-joint section, and a signal charge (electron) corresponding to incoming light volume is accumulated in n-type silicon layer 118, and in p^--type silicon layer 112 converted from an n-type layer. Here, p^+ silicon layer 119 on the topmost surface is for preventing charge leakage from the surface.

[0006] The above-mentioned signal charge accumulation region made from n-type silicon layer 118, etc., is surrounded from the side and

from the bottom by p-type surface-side well 111 formed below and around the element-isolating structure 107, p-type deep well 108 formed at a deep position of the substrate, and long p-type plug well 110 which is formed below element-isolating structure 107 in the up/down direction for electrically connecting p-type surface-side well 111 and p-type deep well 108. With these, the signal charge accumulation region is electrically isolated from surrounding elements in the substrate also, and the signal charge does not leak out.

[0007] Next, major points of the manufacturing method of the photodiode shown in Figure 9 are explained.

[0008] First, element-isolating structure 107 with a LOCOS structure is formed in the peripheral area of light-receiving region 114 of n-type silicon substrate 101 by thermal oxidation of substrate 101.

[0009] Next, using thermal diffusion and anneal treatment by B^+ ion injection and heating, p-type deep well 108 is formed at a deep position of the substrate, p-type plug well 110 is formed below the element-isolating structure 107, and p-type surface-side well 111 is formed below and around element-isolating structure 107. This p-type surface-side well 111 is formed, for a reason mentioned later, so that it covers the edge of element-isolating structure 107 with a LOCOS structure (it protrudes on the side of the light-receiving region 114) by about 0.1 μm . At this time, due to thermal diffusion

from the surrounding p-type region, the n-type layer located below n-type silicon layer 118 is converted to p^--type, forming a p^--type silicon layer 112 surrounded by the p-type well.

[0010] Next, n-type silicon layer 118 is formed at the sensor opening section 115 by As^+ ion injection and thermal anneal treatment. In this manner, a pn-junction (photodiode) is formed at the bordering surface between the silicon layer 112 converted into p^--type and n-type silicon layer 118. Finally, p^+-type silicon layer 119 is formed at the sensor opening section 115 by BF_2^+ ion injection and thermal anneal treatment.

[0011] [History Leading Up to the Invention]

The photodiode shown in Figure 9 has a problem, in terms of miniaturization and high degree of integration, with existence of section 116 protruding from p-type surface-side well 111 by about 0.1 μm width to the light-receiving side 114 at the end of element-isolating structure 107 of the LOCOS structure (Figure 9(b)).

[0012] When element-isolating structure 107 is formed by thermal oxidation of the substrate, a surrounding region 120 with large distortion is created due to bird's beak. Such border region 120 tends to trigger electric charge leak caused by lattice imperfection of the crystal and interface state. In order to prevent such electric charge leaks, the photodiode in Figure 9 forms p-type surface-side well 111 that protrudes on the light-receiving region 114 so that it

wraps the border region 120, thereby isolating the border region 120 from the signal charge accumulation region 118.

[0013] When such protruding section 116 exists, the sensor opening section 115 would become smaller than light-receiving region 114 accordingly. This reduces the sensor opening rate, the area percentage of sensor opening section 115 in unit pixels, and can cause deterioration of photodiode sensitivity. The decrease in the sensor opening rate due to the protruding section 116 would become relatively larger as the area of unit pixels gets smaller to attain higher precision, which would be a great obstacle to miniaturization of the photodiode.

[0014] As a way to resolve the above-mentioned problem, this inventor has proposed a photoelectric converter with a structure in which formation of an element-isolating structure for isolating the photodiodes from each other would not lead to deterioration of photodiode sensitivity easily, and its manufacturing method (JP-A (Tokugan) 2002-118746).

[0015] Namely, the invention relating to JP-A (Tokugan) 2002-118746 ("previously proposed invention" hereafter) relates to a photoelectric converter having a photodiode formed in each light-receiving region, also having a first conductivity-type semiconductor substrate, an element-isolating structure formed on the semiconductor substrate that is formed by a concave section with buried insulating film for isolating photodiodes from each other, a second

conductivity-type channel stopper layer formed in the semiconductor substrate so that it contacts with and surrounds the element-isolating structure, a first conductivity-type semiconductor layer making up the photodiode which is formed on the surface of light-receiving region, a second conductivity-type semiconductor formed at the lower section of and contacting with the first conductivity type semiconductor layer, a second conductivity first well formed to surround the light-receiving region from outside of the light-receiving region and against the element-isolating structure on the light-receiving region side, and second conductivity-type second well formed at the bottom section of the light-receiving region; and also relates to its manufacturing method of said photoelectric converter.

[0016] Figure 2 is a skeleton cross-sectional view (a) and a skeleton top view (b) of a photodiode section such as a CMOS (Complementary Metal Oxide Semiconductor) image sensor, being a preferred embodiment of a previously proposed invention. An element-isolating structure 7b with an STI (Shallow Trench Isolation) structure, for electrically insulating light-receiving region 14 of each photodiode and for isolating photodiodes from each other, is formed on the surface of the substrate.

[0017] In this example, n-type silicon substrate 1 is used for the substrate, and photodiode (PD) is formed by pn-bonding an n-type silicon layer 18 formed on the substrate surface and a silicon layer 12 converted to p^--type below it at their boundary. Hereafter, the

section surrounded by element-isolating structure 7b is called a light-receiving region 14, and its section with a pn-joint is called sensor opening section 15, for distinction.

[0018] Light entering the sensor opening section 15 is converted into an electron hole and electron when it reaches the pn-joint section, and signal charge (electron) corresponding to incoming light volume is accumulated in n-type silicon layer 18, and also in p^--type silicon layer 12 converted from an n-type layer. Here, p^+-type silicon layer 19 on the topmost surface is for preventing charge leakage from the surface.

[0019] The above-mentioned signal charge accumulation region made from n-type silicon layer 18, etc., is surrounded from the side and from the bottom by a p^+-type channel stopper layer 6 formed around the element-isolating structure 7b, p-type surface-side well 11 formed below the element-isolating structure 7b, p-type deep well 8 formed at a deep position of the substrate, and long p-type plug well 10 which is formed below the element-isolating structure 7b in up/down direction for electrically connecting p-type surface-side well 11 and p-type deep well 8. With these, the signal charge accumulation region is electrically isolated from surrounding elements in the substrate also, and the signal charge would not leak out.

[0020] The border between p-type surface-side well 11 and p-type plug well 10 and layer 12 converted to p^--type is formed at a position which is set back from immediately below the STI terminal by 0.2 μm

as seen from light-receiving region 14. This is to increase the signal charge accumulation capacity.

[0021] When Figure 2(b) and Figure 9 (b) are compared, it is possible to clearly understand the photodiode under the preferred embodiment of the previously proposed invention and a conventional photodiode example. In Figure 2 (b), since p^+-type channel stopper layer 6 is formed contacting the STI element-isolating structure 7b, p-type layer 116 protruding into light-receiving region 114 shown in Figure 9 (b) is no longer necessary.

[0022] Although a border region with large distortion is formed around the STI element-isolating structure 7b also, since it is possible to form p^+-type channel stopper layer 6 in the border region by ion injection from the wall of the concave section after the concave section is formed, this would allow creating a thinner p^+-type channel stopper layer 6 compared to p-type layer 116 in the LOCOS structure, where the thickness of this thinner p^+-type channel stopper layer 6 would be equal to or less than 0.1 μm, about 30 nm for example.

[0023] In this manner, almost the entire area of light-receiving region 14, surrounded by the element-isolating structure 7b, is the sensor opening section 15. Thus, the area of sensor opening section 15 can be increased over the conventional one by the amount saved by the protruding section 116 of the p-type surface-side well, improving the sensitivity of the photodiode.

[0024] Further, compared to LOCOS structure 107, etc., since STI structure 7b can significantly narrow down the width of the insulating material for element isolation, the area of the element-isolating structure itself can be decreased.

[0025] Thus, the sensor opening rate, being the rate of sensor opening section 15 area in unit pixels, can be increased, improving the sensitivity of the photodiode.

[0026] Further, silicon layer 12 converted into p^--type that is expanded to the outside of light-receiving region 14, as against immediately below the terminal of element-isolating structure 7b, can be used as part of the signal charge accumulation region. Thus, even when a large amount of light should generate a large amount of signal charge, it is possible to accumulate the signal charge without getting saturated, enabling a large dynamic range.

[0027] Next, major points of the manufacturing method of the photodiode of the image sensor shown in Figure 2 are explained.

[0028] First of all, a concave section is formed around the light-receiving region 14 using selective etching. Then, the inside wall of the concave section is thermally oxidized to form a thin oxide silicon film on the inside wall of the concave section.

[0029] Then, prior to burying the concave section with oxide silicon, BF_2^+ ion is injected from the inside wall of the concave section at a 30-degree tilt against the substrate vertical at an acceleration voltage of 100 keV and an injection amount (surface

density) of 2 x $10^{13}/cm^2$. This would form p^+-type channel stopper layer 6 on the side wall and bottom surface of the concave section.

[0030] Next, after burying the oxide silicon in the concave section, excess oxide silicon is removed and STI element-isolating structure 7b is formed.

[0031] Then, the entire pixel region is treated including the light-receiving region 14 for thermal diffusion and anneal treatment by B^+ ion injection and heating at acceleration voltage of 2 Me V, forming a p-type deep well 8 at a deep position of the substrate. Then, while masking the light-receiving region 14 and part of STI element-isolating structure 7b, the pixel region is treated for thermal diffusion and anneal treatment by B^+ ion injection and heating at an acceleration voltage of 1.5 Me V and 1.0 Me V, forming p-type plug well 10.

[0032] Then, in a similar manner, while masking the light-receiving region 14 and part of STI element-isolating structure 7b, using thermal diffusion and anneal treatment by B^+ ion injection and heating at an acceleration voltage of 600 keV, 380 keV, and 190 keV, forming p-type surface-side well 11.

[0033] By forming the p-type surface-side well 11, the signal charge accumulating region of a photodiode such as n-type silicon layer 18 is separated from an other n-type silicon region of the substrate. Further, normally, p-type surface-side well 11 is also formed at the peripheral circuit section other than the pixel region

as a p-type well of a semiconductor circuit element of a peripheral circuit.

[0034] At this time, due to thermal diffusion during the formation process of a series of p-type wells, the n-type layer located below the n-type silicon layer 18 is converted to p^--type, forming a p^--type silicon layer 12 surrounded by the p-type well.

[0035] Next, n-type silicon layer 18 is formed at the sensor opening section 15 by As^+ ion injection and thermal anneal treatment under acceleration voltage of 300 keV. In this manner, a pn-junction (photodiode) is formed at the bordering surface between the silicon layer 12 converted into p-type and the n-type silicon layer 18.

[0036] Finally, p^+-type silicon layer 19, which prevents a signal charge leakage from the surface, is formed at the light-receiving region 14 by BF_2^+ ion injection and a thermal anneal treatment at acceleration voltage of 50 keV.

[0037] [Problems to be Resolved by the Invention]

Figure 1 (b) is a conceptual skeleton cross-sectional view of a completed CMOS image sensor. At the top section of the drawing, we have added a skeleton cross-sectional view showing the formation process of p^+ channel stopper layer 6 by injecting BF_2^+ ion into the substrate from the inside wall of concave section 4, among the manufacturing process of above-mentioned photodiode.

[0038] As can be seen in this drawing, in this example, ion injection to the inside wall of concave section 4 is performed

against all of concave section 4 on the substrate 1 without distinguishing photodiode section. For this reason, p+ channel stopper layer 6 with same density is formed in the substrate surrounding all of concave section 4 of the substrate 1.

[0039] However, normally the p^+ layer is not formed on the STI side wall of the peripheral circuit section. Even if such is to be formed, its optimal dopant density is much smaller than the optimal dopant density of the p^+ layer at the channel stopper layer of the photodiode section. Thus, since optimal conditions differ between these two, if p^+ channel stopper layer 6 is formed uniformly as above, the property of the transistor and another element of the peripheral circuit and the property of the transistor in pixels would change, and there is a danger to adversely influence driving of the sensor.

[0050] As explained above, although p^+ channel stopper layer 6 based on the previously proposed invention and its formation method are effective for improving photodiode sensitivity, it was found that there is room for improvement of the relationship with the semiconductor elements around the photodiode.

[0041] This invention is proposed in view of the above observation, and its objective is to provide a photoelectric converter having an element-isolating structure for isolating photodiodes from each other whose formation causes little deterioration of the sensitivity of photodiodes and does not have an

adverse influence on the peripheral semiconductor elements, and to provide its manufacturing method.

[0042] [Means of Solving the Problems]

This invention relates to a photoelectric converter having photodiodes formed on the respective light-receiving region on the first conductivity-type semiconductor substrate, and semiconductor circuit elements formed in regions other than said light-receiving regions on said semiconductor substrate; further having an element-isolating structure formed on said semiconductor substrate, which has an insulating film buried in a concave section, for isolating elements between said photodiodes and said semiconductor circuit elements; a second conductivity-type channel stopper layer formed in said semiconductor substrate which contacts and surrounds said element-isolating structure for isolating said photodiodes; first, a conductivity-type semiconductor layer, formed on the front side of said light-receiving region, that constitutes said photodiode; a second conductivity-type first well, formed at the outside position of said light-receiving region against the edge of said element-isolating structure on said light-receiving region side, so as to surround said light-receiving region; a second conductivity-type second well formed at the bottom section of said light-receiving region; and a second conductivity-type third well which connects said first and second wells; wherein said channel stopper layer terminates at a specific position in said first well contacting with and

surrounding said element-isolating structure and between the peripheral area of said light-receiving region and said semiconductor circuit element.

[0043] Further, this invention relates to a manufacturing method of the photoelectric converter, which forms photodiodes on the respective light-receiving region on the first conductivity-type semiconductor substrate, and forms semiconductor circuit elements in regions other than said light-receiving regions on said semiconductor substrate; having a process that forms a concave section for isolating said photo diode and said semiconductor circuit element, and forms an element-isolating structure by burying insulating film in this concave section; a process that forms a second conductivity-type channel stopper layer, in said semiconductor substrate which contacts and surrounds said element-isolating structure, for isolating said photodiodes; a process for forming a first conductivity-type semiconductor layer on the front side of said light-receiving region that constitutes said photodiode; a process to form a second conductivity-type first well, at the outside position of said light-receiving region against the edge of said element-isolating structure on said light-receiving region side, so as to surround said light-receiving region; a process to form a second conductivity type second well at the bottom section of said light-receiving region; and a process to form a second conductivity-type third well which connects said first and second wells; wherein said

channel stopper layer terminates at a specific position in said first well contacting with and surrounding said element-isolating structure and between the peripheral area of said light-receiving region and said semiconductor circuit element.

[0044] Under this invention, although a bordering region with large distortion is also formed around the above-mentioned element-isolating structure, since it is possible after formation of said concave section to form said second conductive-type channel stopper layer at the said bordering region by impurity doping from said concave section, it is possible to make the channel stopper layer thinner compared to a LOCOS structure, to increase the sensor opening rate being the area percentage of the sensor opening section in the unit pixels, and to improve sensitivity of the photodiode.

[0045] Further, since said channel stopper layer terminates around said light-receiving region and at a position between said semiconductor circuit element, the formation of said channel stopper layer cannot adversely influence said semiconductor circuit element.

[0046] [Mode of Implementation of this Invention]

In this invention, it is desired that said element-isolating structure is provided at least around said light-receiving region.

[0047] It is desired that said element-isolating structure is an STI (Shallow Trench Isolation) structure. Further, compared to LOCOS structure, etc., since said STI structure can significantly narrow

down the width of the insulating material for element isolation, the area of the element-isolating structure itself can be decreased.

[0048] In this invention, it is desirable to form said channel stopper layer of the photodiode section, after said concave section is formed and prior to burying said insulating film in said concave section, by injecting ion from the wall surface of said concave section of photodiode section while masking peripheral area of photodiode other than said photodiode section.

[0049] It is acceptable that said element-isolating structure is provided between said photodiode in said light-receiving region and said semiconductor circuit element in surrounding non-light-receiving section, and/or between said semiconductor circuit element in said non-light-receiving section and said semiconductor element in surrounding circuit section.

[0050] In this case, it is desirable that said first well is also formed in regions of said semiconductor circuit element of said non-light-receiving section and/or said semiconductor circuit element of said peripheral circuit section, and a channel stopper layer of lower density than previously mentioned channel stopper layer of said photodiode section is also formed in said first well adjacent to said element-isolating structure around said semiconductor circuit element.

[0051] By forming the channel stopper layer of said semiconductor circuit element section separate from the channel stopper layer of

said photodiode section, it is possible to form channel stopper layers having their own optimal impurity density.

[0052] In this invention, it is desirable that, after said concave section is formed and prior to burying said insulating film in said concave section, said channel stopper layer of said semiconductor circuit element section is formed by injecting ion from the wall surface of said concave section while masking photodiode section and semiconductor circuit element section of said non-light-receiving section and/or semiconductor circuit element section of said peripheral circuit section.

[0053] Further, when forming said element-isolating structure, it is desirable that insulating material for isolating elements is buried in said concave section by a vapor growth method.

[0054] It is desirable that said first, second, and third wells are formed by an ion injection method. With the ion injection method, it is possible to accurately conduct doping at a prescribed location with desired density. For this reason, it is possible to form a well in a deep section of said semiconductor substrate, which is not possible by a thermal diffusion method, for example.

[0055] It is desirable that a solid-state photographing device is manufactured based on this invention.

[0056] Desirable embodiments of this invention are explained next in detail using illustrating drawings as reference.

[0057] Embodiment 1: CMOS image sensor (1)

Figure 2 is a skeleton cross-sectional view (a) and a skeleton top view (b) of a photodiode section of a CMOS (Complementary Metal Oxide Semiconductor) image sensor, being a preferred embodiment of this invention. An element-isolating structure 7b with an STI (Shallow Trench Isolation) structure, for electrically insulating light-receiving region 14 of each photodiode and for isolating photodiodes from each other, is formed on the surface of the substrate.

[0058] In this example, n-type silicon substrate 1 is used for the substrate, and photodiode is formed by pn-bonding an n-type silicon layer 18 formed on the upper section of the substrate and a silicon layer 12 below, converted to p^--type, at their boundary.

[0059] Light entering the sensor opening section 15 of light-receiving region 14 is converted into electron hole and electron when it reaches the pn-joint section, and a signal charge (electron) corresponding to incoming light volume is accumulated in n-type silicon layer 18, and in p^--type silicon layer 12 converted from the n-type layer. Here, p^+ silicon layer 19 on the topmost surface is for preventing charge leakage from the surface.

[0060] The signal charge accumulation region made from n-type silicon layer 18 is surrounded from the side and from the bottom by a p^+-type channel stopper layer 6 formed around the element-isolating structure 7b, a p-type surface-side well 11 formed below the element-isolating structure 7b, a p-type deep well 8 formed at a deep

position of the substrate, and along p-type plug well 10 which is formed below the element-isolating structure 7b in the up/down direction for electrically connecting p-type surface-side well 11 and the p-type deep well 8. With these, n-type signal charge accumulation region 18 is electrically isolated from surrounding elements in the substrate also, and the signal charge would not leak out.

[0061] The border between p-type surface-side well 11 and p-type plug well 10 and layer 12 converted to p^--type is formed at a position which is set back from immediately below STI terminal by 0.2 μm as seen from light-receiving region 14. This is to increase the signal charge accumulation capacity.

[0062] Since the structure of the above photodiode is the same as the photodiode under the previously proposed invention, it goes without saying that it would result in the same effect.

[0063] Namely, since p^+-type channel stopper layer 6 is formed contacting STI element-isolating structure 7b, p-type layer 116 protruding into light-receiving region 114 shown in Figure 9 (b) is no longer necessary.

[0064] Although a border region with large distortion is formed around STI element-isolating structure 7b also, since it is possible to form p^+-type channel stopper layer 6 in the border region by ion injection from the wall of the concave section after the concave section is formed, this would allow creating a thinner p^+-type channel stopper layer 6 compared to p-type layer 116 in the LOCOS structure,

where the thickness of this thinner p^+-type channel stopper layer 6 would be equal to or less than 0.1 μm, about 30 nm for example.

[0065] In this manner, almost the entire area of the light-receiving region 14, surrounded by the element-isolating structure 7b, is the sensor opening section 15. Thus, the area of sensor opening section 15 can be increased, improving the sensitivity of the photodiode.

[0066] Further, compared to LOCOS structure 107, etc., since STI structure 7b can significantly narrow down the width of the insulating material for element isolation, the area of element-isolating structure itself can be decreased.

[0067] Thus, the sensor opening rate, being the rate of sensor opening section 15 area in unit pixels, can be increased, improving the sensitivity of the photodiode.

[0068] Further, silicon layer 12 converted into a p^--type that is expanded to the outside of light-receiving region 14, as against immediately below the terminal of element-isolating structure 7b, can be used as part of a signal charge accumulation region. Thus, even when a large amount of light should generate a large amount of signal charge, it is possible to accumulate the signal charge without getting saturated, enabling a large dynamic range.

[0069] Figure 3 is a skeleton block diagram showing composition of a CMOS image sensor where the above-mentioned photodiode is set on the substrate in a two-dimensional matrix shape. In this device, the

column and row are selected by vertical scanner 32 and horizontal scanner 34, respectively, and the signal charge of the photodiode of pixel 31 at their intersection is read.

[0070] Namely, when a reader transistor 33 of a certain column is selected by a control signal from vertical scanner 32 and is turned ON, and at the same time a read signal is added in sequence to each row by a horizontal scanner, output from pixel 31 at the intersection is fed to the input section of current-voltage converter circuit 35, where the output is converted to voltage by current-voltage converter circuit 35 and output buffer circuit 36, and is outputted.

[0071] All pixel 31 is scanned once in sequence during one cycle of vertical scanner 32, and output corresponding to signal charge that was accumulated in photodiode of each pixel 31 during one cycle is read out, and at the same time, charge is eliminated from the photodiode, resetting to the initial state. In this manner, photodiode arranged in two-dimensional matrix shape performs photoelectric conversion, outputting time-sliced image signals.

[0072] Each pixel 31 in Figure 3 is formed in pixel region 37 on the substrate, while vertical scanner 32, reader transistor 33, horizontal scanner 34, current-voltage converter circuit 35, and peripheral circuits such as output buffer circuit 36 are formed in peripheral circuit section 38 next to pixel region 37.

[0073] Figure 4 is a top view showing layout in pixel region 37. Figure 4 (a) is an overall diagram showing how the plurality of pixel

31 is laid out in a two-dimensional matrix shape, while Figure 4 (b) is a top view showing a layout in a single pixel 31. Figure 4 only shows n-type diffusion layer 18 and 43 formed on the top section of the p-type silicon layer; gate layer 42, 45, and 48; and contact 41, 44, and 49, etc. Top layer wiring is omitted from the figure. The gate layer is formed from polycrystalline silicon, and its lower section is a p-type layer.

[0074] N-type silicon layer 18 shown in Figure 4 (b) forms a photodiode by pn-bonding at the border of n-type silicon layer 18 and silicon layer 12 below which was converted to p^--type, as was explained in Figure 2, generating signal charge (electron) corresponding to the light amount of incoming light. This signal charge (electron) is accumulated during one cycle in the signal charge accumulation region, mainly in n-type region 18.

[0075] Read signal from horizontal scanner in Figure 3 is added to transfer gate 42 via contact 41 in Figure 4. When a read signal changes the channel layer below the transfer gate 42 to a conductive state, signal charge (electron) accumulated in signal charge accumulating region of n-type silicon, etc. is transferred to n-type buffer layer 43 formed in non-light-receiving section in the pixel, and generates signal voltage corresponding to the signal charge amount.

[0076] This signal voltage is applied to gate 45 of amplifier transistor via contact 44, which is read as a change in current

flowing in the amplifier transistor 46. The output current of the amplifier transistor 46 is fed to reader transistor 33 in Figure 33, and is converted into voltage as explained before and is outputted.

[0077] When reading is completed, reset signal is applied to reset gate 48 via contact 47, signal charge stored in n-type buffer layer 43 is eliminated via contact 49, and the photodiode is reset to the initial state.

[0078] As explained above, a single pixel contains a photodiode formed in the light-receiving section and various semiconductor circuit elements formed in the non-light-receiving section. Thus, it is necessary to isolate pixels from each other and also isolate elements from each other in one pixel.

[0079] Spread in n-type silicon layer 18 in Figure 4 corresponds to sensor opening section 15 (Figure 2). Thus, the end section 50A, on the light-receiving side of p^+ channel stopper layer 6 formed adjacent to the STI element-isolating structure of the photodiode section, is on the periphery (solid line) of n-type silicon layer 18. The other end section 50B is at the location indicated by a broken line, and terminates between amplifier transistor 46 formation region of non-light-receiving section.

[0080] Figure 1 (a) is a conceptual skeleton cross-sectional view of the CMOS image sensor, whose peripheral circuit section is cut off first, then the non-light-receiving section of the pixel (A-B of Figure 4 (b), for example) is cut off, then the light-receiving

section of the pixel (B-C of Figure 4 (b), for example), yielding the cross-sectional diagram that connects all of the above.

[0081] At the top section of Figure 1 (a), we have added a skeleton cross-sectional view showing the formation process of p^+ channel stopper layer 6 by injecting BF_2^+ ion into the substrate from the inside wall of concave section 4, among the manufacturing process of the CMOS image sensor to be mentioned later.

[0082] As can be seen in the figure, since the semiconductor circuit element section of the non-light-receiving section and semiconductor circuit element section of peripheral circuit section are covered by mask 30 when BF_2^+ ion is injected, p^+ channel stopper layer 6 is formed only below the STI element-isolating structure of photodiode section and the p^+ channel stopper layer 6 ends at a middle position 50B of the STI element-isolating structure and semiconductor circuit element section of the pixel region non-light-receiving section and does not extend to its semiconductor circuit element section. Thus, there is no risk that it can exert adverse influence on transistor 51 in pixel (amplifier transistor 46, etc.), transistor 52 of peripheral circuit section 38, and other elements.

[0083] Although p-type deep well 8 and p-type plug well 10 can be formed only in the light-receiving section, it is normally desirable that it is formed over the entire pixel region from the light-receiving section to the non-light-receiving section. This is to prevent leakage of the signal charge more effectively.

[0084] Further, although p-type surface-side well 11 can be formed only at the light-receiving section, normally it is formed at the same time as the p-type well of s the emiconductor circuit element formed at the peripheral section and the non-light-receiving section. This is to prevent leakage of signal charge more effectively and to form the image sensor efficiently.

[0085] It is desirable that transistors 51 and 52 formed at peripheral circuit section and non-light-receiving section to have LDD (Lightly Doped Drain-source) structure. This would alleviate draining the electric field and improve voltage-proof property.

[0086] Embodiment 2: Manufacturing CMOS image sensor (1)

Figures 5~7 are skeleton cross-sectional views that show the manufacturing process, in the order of the process, of CMOS image sensor (1) shown under Embodiment 1 by the manufacturing method of the photoelectric converter under the preferable embodiment of this invention.

[0087] Process 1: First of all, as shown in Figure 5(a), silicon oxide film 2 and silicon nitride film 3 are laminated and formed on the surface of n-type semiconductor substrate 1 by CVD (Chemical Vapor Deposition) method. Then, these films 2 and 3 are patterned to shapes corresponding to the pattern of concave section 4 of STI structure 7b.

[0088] Process 2: Next, as shown in Figure 5 (b), silicon oxide film 2 and silicon nitride film 3 are used as a mask to remove the

silicon by dry etching (reactive ion etching), etc., to form concave section 4.

[0089] Process 3: Then, as shown in Figure 5 (c), the inside wall of the concave section 4 is thermally oxidized to form a thin oxide silicon film on the inside wall of the concave section 4.

[0090] Process 4: Then, prior to burying the concave section 4 with oxide silicon, as shown in Figure 5 (d), while covering the peripheral circuit section and non-light-receiving section with a mask 30, inject BF_2^+ ion from the inside wall of the concave section 4, at a 30-degree tilt against the substrate vertical, at an acceleration voltage of 100 keV and an injection amount (surface density) of 2 x $10^{13}/cm^2$, to form p^+-type channel stopper layer 6.

[0091] At this time, as was explained in Figure 1 (a), p^+-type channel stopper layer 6 is formed only in the light-receiving section, and it would not adversely affect peripheral circuit section 38 and the semiconductor circuit element formed in the non-light-receiving section.

[0092] Process 5: Next, as shown in Figure 6 (e), oxide silicon 7a is deposited by a CVD (Chemical Vapor Deposition) method, etc., to bury oxide silicon 7a in trench groove 4.

[0093] Process 6: Next, as shown in Figure 6 (f), the surface is polished by CMP (Chemical Mechanical Polishing), etc., excess oxide silicon, nitride silicon film 3, and oxide silicon film 2 are

removed, in that order, to complete STI element-isolating structure 7b.

[0094] Process 7: Then, as shown in Figure 6 (g), while covering peripheral circuit section 38 by mask 21, B^+ ion is injected over the entire pixel region 37 including the light-receiving region 14 at an acceleration voltage of 2 Me V and an injection amount (surface density) of 5 x $10^{11}/cm^2$, followed by thermal diffusion and anneal treatment by heating, forming p-type deep well 8 at a deep position of the substrate.

[0095] Process 8: Then, as shown in Figure 6 (h), while covering peripheral circuit section 38 and light-receiving region 14 and part of STI element-isolating structure 7b by mask 9, B^+ ion is injected beneath STI structure 7b at an acceleration voltage of 1.5 Me V and an injection amount (surface density) of 8 x $10^{11}/cm^2$, and an acceleration voltage of 1.0 Me V and a surface density of 3 x $10^{12}/cm^2$, followed by thermal diffusion and anneal treatment by heating, forming a p-type plug well 10.

[0096] Although p-type deep well 8 and p-type plug well 10 can be formed only in the light-receiving section, it is normally desirable that it is formed over the entire pixel region 37 from the light-receiving section to non-light-receiving section. This is to prevent leakage of signal charge more effectively.

[0097] Process 9: Then, as shown in Figure 7 (i), while covering light-receiving region 14 and part of STI element-isolating structure

7b by mask 32, B^+ ion is injected at an acceleration voltage of 600 keV and an injection amount (surface density) of 3 x $10^{12}/cm^2$; an acceleration voltage of 380 keV and a surface density of 3 x $10^{12}/cm^2$; and acceleration voltage of 190 keV and an injection amount (surface density) of 6 x $10^{12}/cm^2$, followed by thermal diffusion and anneal treatment by heating, forming p-type surface-side well 11.

[0098] By forming the p-type surface-side well 11, the n-type silicon layer of light-receiving region 14 is separated from other n-type silicon region. Although p-type surface-side well 11 can be formed only at the light-receiving section, normally it is formed at the same time as the p-type well of the semiconductor circuit element formed at peripheral section 38 and non-light-receiving section. This is to prevent leakage of the signal charge more effectively and to form the image sensor efficiently.

[0099] At this time, the n-type silicon layer is converted to p^--type due to thermal diffusion during well formation, forming a silicon layer 12 converted to p^--type surrounded by the p-type well.

[0100] Process 10: Then, as shown in Figure 7 (j), while masking sections other than sensor opening section 15, As^+ ion is injected into sensor opening section 15 at an acceleration voltage of 300 keV and an injection amount (surface density) of 2 x $10^{12}/cm^2$, followed by heat anneal treatment, forming a n-type silicon layer 18. In this manner, a pn-junction (photodiode) is formed at the bordering surface between the p-type silicon layer 12 and the n-type silicon layer 18.

Thus, as shown in Figure 2 (b), the region surrounded by p^+-type channel stopper layer 6 in the top view would become sensor opening section 15.

[0101] Process 11: Then, as shown in Figure 4 (k), while masking sections other than light-receiving section 14, BF_2^+ ion is injected at an acceleration voltage of 50 keV and a surface density of 1 x $10^{13}/cm^2$, followed by heat anneal treatment, forming p^+-type silicon layer 19.

[0102] Process 12: Finally, after forming oxidation film by thermal oxidation on the peripheral circuit section and the substrate surface of the desired region of the non-light-receiving section, semiconductor circuit elements such as non-light-receiving transistor 51 and peripheral circuit transistor 52 are formed by publicly known method.

[0103] Embodiment 3: CMOS image sensor (2) and manufacturing method

Figure 8 (b) is a conceptual skeleton cross-sectional view of completed CMOS image sensor (2) which is a variation of Embodiment 1. At the top section of the drawing, we have attached a skeleton cross-sectional view showing the formation process of p^+ channel stopper layer 6a, added as a manufacturing process 4a, in which BF_2^+ ion is injected into the substrate from the inside wall of the concave section of peripheral circuit section 38 and the non-light-receiving section.

[0104] In this variation example, the manufacturing process shown in Embodiment 2 is modified so that process 4 (while covering peripheral circuit section 38 and the non-light-receiving section with mask 30, BF_2^+ ion is injected from the inside wall of the concave section 4, at a 30-degree tilt against the substrate vertical, at an acceleration voltage of 100 keV and an injection amount (surface density) of 2 x $10^{13}/cm^2$, to form p^+-type channel stopper layer 6 in the light-receiving section only) is followed by additional process 4a explained below.

[0105] Process 4a: As shown in attached Figure 8 (a), while covering the light-receiving section with mask 30a, BF_2^+ ion is injected from the inside wall of concave section 4, at a 30-degree tilt against the substrate vertical, at an acceleration voltage of 100 keV and an injection amount (surface density) of 1 x $10^{13}/cm^2$, to form p^+-type channel stopper layer 6a on peripheral circuit section 38 and the non-light-receiving section.

[0106] This process forms p^+-type channel stopper layer 6a in the peripheral circuit section 38 and the non-light-receiving section with less density than p^+-type channel stopper layer 6 of the light-receiving section. This density can be set to the optimal density that does not adversely affect semiconductor circuit elements formed in this region.

[0107] Since this is the same as Embodiment 1, except for added p^+-type channel stopper layer 6a, the same effect mentioned in Embodiment 1 can naturally be obtained in Embodiment 3.

[0108] Embodiment 4 : CMOS image sensor (3) and manufacturing method

Figure 8 (b) is a conceptual skeleton cross-sectional view of CMOS image sensor (3) which is yet another variation of Embodiment 1. At the top section of the drawing, we have attached a skeleton cross-sectional view showing the formation process of p^+ channel stopper layer 6b, added as a manufacturing process 4b, in which BF_2^+ ion is injected into the substrate from the inside wall of the concave section of the non-light-receiving section.

[0109] In this variation example, the manufacturing process shown in Embodiment 2 is modified so that the process 4 (while covering the peripheral circuit section 38 and non-light-receiving section with a mask 30, BF_2^+ ion is injected from the inside wall of the concave section 4, at a 30-degree tilt against the substrate vertical, at an acceleration voltage of 100 keV and an injection amount (surface density) of $2 \times 10^{13}/cm^2$, to form p^+-type channel stopper layer 6 in the light-receiving section only) is followed by additional process 4b explained below.

[0110] Process 4a: As shown in attached Figure 8 (b), while covering the peripheral circuit section 38 and the light-receiving section with a mask 30b, inject BF_2^+ ion from the inside wall of the concave section 4, at a 30-degree tilt against the substrate

vertical, at an acceleration voltage of 100 keV and an injection amount (surface density) of 1 x $10^{13}/cm^2$, to form p^+-type channel stopper layer 6b in non-light-receiving section.

[0111] This process forms p^+-type channel stopper layer 6b in the non-light-receiving section only with less density than p^+-type channel stopper layer 6 of the light-receiving section. This density can be set to the optimal density that does not adversely affect semiconductor circuit elements formed in this region.

[0112] Normally, since the element-isolating structure of the non-light-receiving section is in contact with p-type well, electric charge can easily leak. Thus, providing p^+-type channel stopper layer 6b in the non-light-receiving section has a significant effect. Further, ion injection can also add a favorable effect since it allows adjusting threshold value voltage V_{TH} and current characteristic I_D of transistors.

[0113] Since this is the same as Embodiment 1, except for added p^+-type channel stopper layer 6b, the same effect mentioned in Embodiment 1 can naturally be obtained in Embodiment 4.

[0114] This completes the explanation of embodiments of this invention. However, this invention is not limited by these examples and can naturally be modified appropriately as long as such modification does not depart from the spirit of this invention.

[0115] For example, ion injection for forming wells mentioned above could be carried out prior to formation of the STI element-

isolating structure. Further, conductivity types of each semiconductor region mentioned above could be reversed. Further, element isolation of peripheral circuit section 38 could be realized by a method other than the STI structure.

[0116] [Advantageous effect of invention]

Under this invention, although a bordering region with large distortion is formed around the above-mentioned element-isolating structure, since it is possible after formation of said concave section to form said second conductivity type channel stopper layer at the said bordering region by impurity doping from said concave section, it is possible to make the channel stopper layer thinner compared to the LOCOS structure, to increase the sensor opening rate being the area percentage of the sensor opening section in the unit pixel, and to improve the sensitivity of photodiode.

[0117] Further, compared to the LOCOS structure etc., since the STI structure can significantly narrow down the width of the insulating material for element isolation, the area of the element-isolating structure itself can be decreased.

[0118] Thus, the sensor opening rate, being the percentage of the sensor opening section area in unit pixels, can be increased, improving the sensitivity of the photodiode.

[0119] Further, since said channel stopper layer terminates around said light-receiving region and at a position between said

semiconductor circuit elements, the formation of said channel stopper layer cannot adversely influence semiconductor circuit elements.

[Brief Description of the Figures]

[Figure 1] A skeleton cross-sectional view of the CMOS image sensor which is a preferred embodiment of this invention and the previously proposed invention.

[Figure 2] A skeleton cross-sectional view (a) and a skeleton top view (b) of a photodiode section of a CMOS image sensor, being a preferred embodiment of the previously proposed invention and this invention.

[Figure 3] A block diagram of CMOS image sensor under an embodiment of this invention.

[Figure 4] A top view showing the layout in the pixel region under the same.

[Figure 5] A skeleton cross-sectional view showing the manufacturing process of CMOS image sensor under the same.

[Figure 6] A skeleton cross-sectional view showing the manufacturing process of the CMOS image sensor under the same.

[Figure 7] A skeleton cross-sectional view showing the manufacturing process of the CMOS image sensor under the same.

[Figure 8] A skeleton cross-sectional view of the CMOS image sensor which is another preferred embodiment of this invention.

[Figure 9] A skeleton cross-sectional view (a) and a skeleton top view (b) of a photodiode section of cthe onventional image sensor.

[Explanation of codes]

1 … n-type semiconductor substrate;

2 … Silicon oxide film;

3 … Silicon nitride film;

4 … Concave section;

5 … Silicon oxide film;

6 … p^+-type channel stopper layer;

7a … Silicon oxide;

7b … Element-isolating structure (STI structure);

8 … p-type deep well;

9 … Mask;

10 … p-type plug well;

11 … p-type surface-side well;

12 … Silicon layer converted to p^--type;

13 … Mask;

14 … Light-receiving region;

15 … Sensor opening section;

18 … n-type silicon layer;

19 … p^+-type silicon layer;

20, 21, 30, 30a, 30b … Mask;

31 … Pixel;

32 … Vertical scanner;

33 … Reader transistor;

34 … Horizontal scanner;

35 … Current-voltage converter circuit;

36 … Output buffer circuit;

37 … Pixel region;

38 … Peripheral circuit section;

41 … Contact;

42 … Transfer gate;

43 … n-type buffer layer;

44 … Contact;

45 … Amplifier transistor gate;

46 … Amplifier transistor;

47 … Contact;

48 … Reset gate;

49 … Contact;

50A … p^+-type channel stopper layer light-receiving region side end;

50B … Other end of p^+-type channel stopper layer;

51 … Non-light-receiving section transistor;

52 … Peripheral circuit section transistor;

101 … n-type semiconductor substrate;

102 … Silicon oxide film;

107 … Element-isolating structure (LOCOS structure);

108 … p-type deep well;

110 … p-type plug well;

111 … p-type surface-side well;

112 … Silicon layer converted to p^--type;

114 … Light-receiving region;

115 … Sensor opening section;

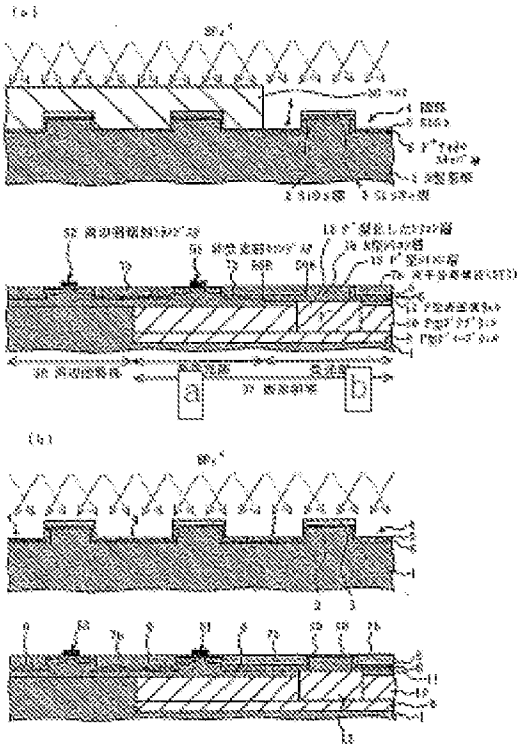
116 … Protrusion from p-type surface-side well;

118 … n-type silicon layer;

119 … p^+-type silicon layer;

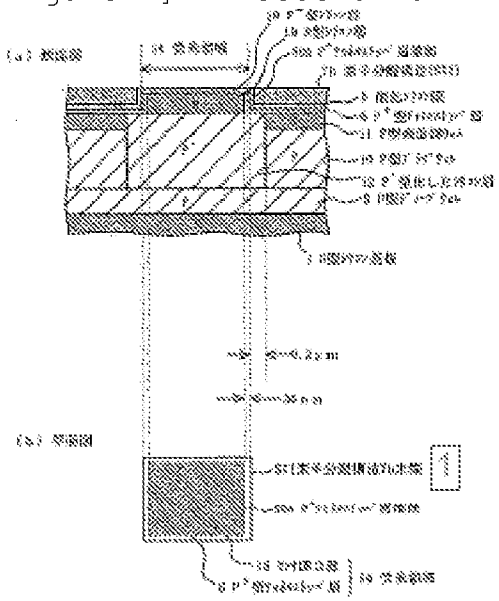
120 … Border region with large distortion.

[Figure 1] Example of CMOS image sensor



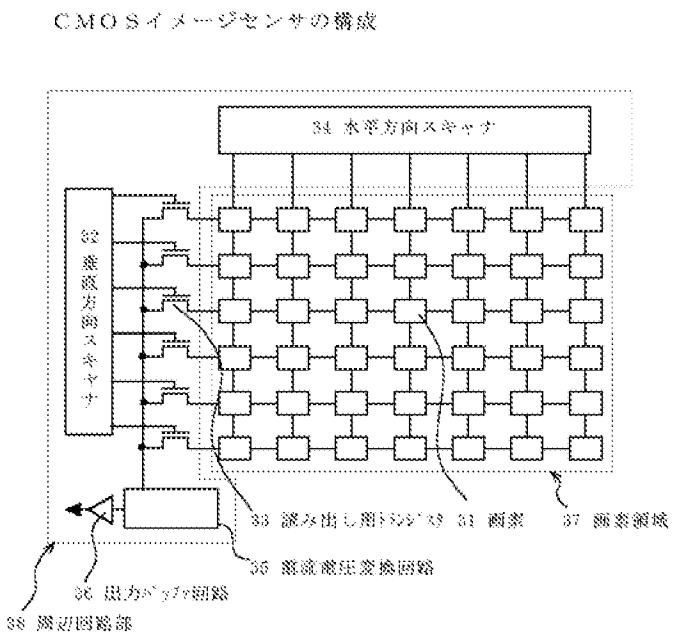
Key:
a) Non-light-receiving section
b) Light-receiving section

[Figure 2] PD section of image sensor

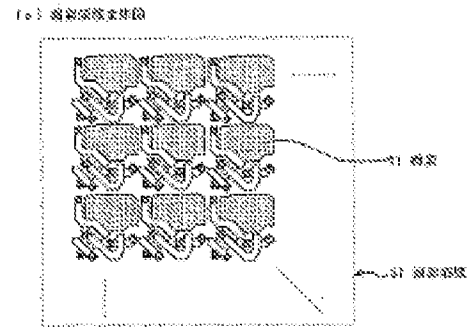


Key:
(a) Cross-sectional view
(b) Top view
1) End of STI element-isolating structure 7b

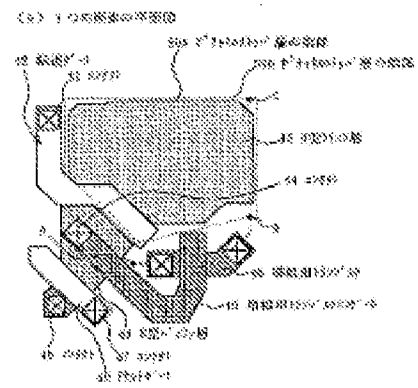
[Figure 3]Composition of CMOS image sensor



[Figure 4]

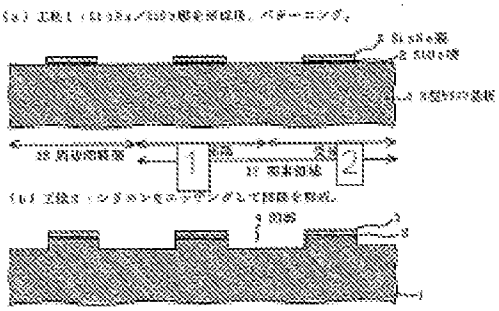


(a) Overall view of pixel region



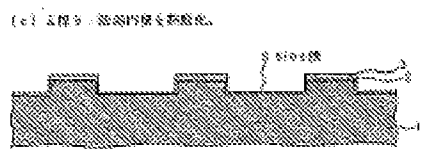
(b) Top view of single pixel

[Figure 5] Production process of image sensor

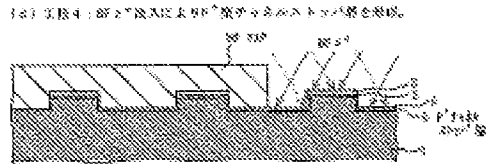


(a) Process 1: After forming Si_3N_4/SiO_2 film, patterning
1) Non-light-receiving section
2) Light-receiving section

(b) Process 2: Concave section formed by etching silicon

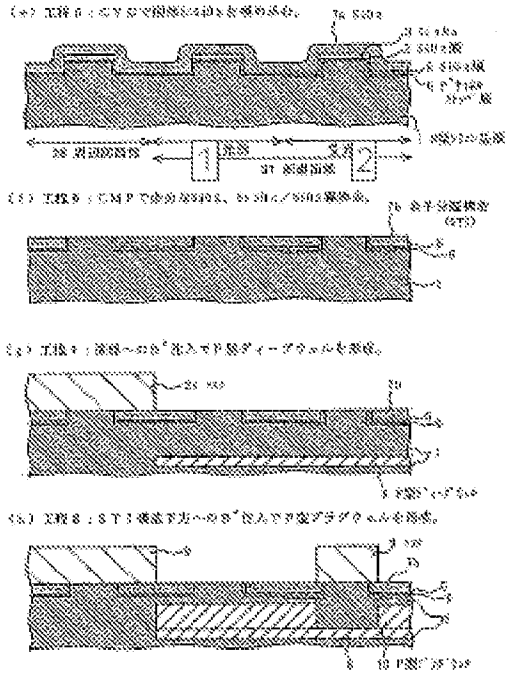


(c) Process 3: Thermal oxidation of inside wall of concave section



(d) Process 4: BF_2^+ injected to form p^+-type channel stopper layer

[Figure 6] Production process of image sensor



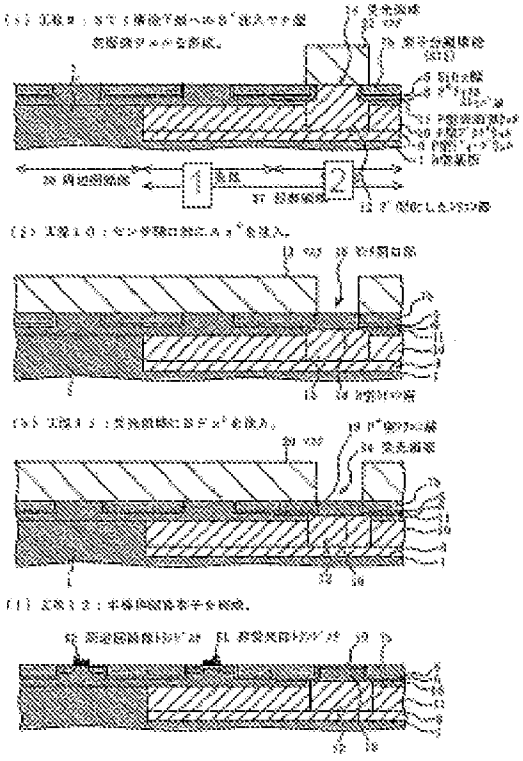
(e) Process 5: SiO_2 buried in concave section by CVD
1) Non-light-receiving section
2) Light-receiving section

(f) Process 6: Excess SiO_2, Si_3N_4/SiO_2 film removed by CMP

(g) Process 7: B^+ injected into deep section to form p-type deep well

(h) Process 8: B^+ injected to below STI structure to form p-type plug well

[Figure 7] Production process of image sensor



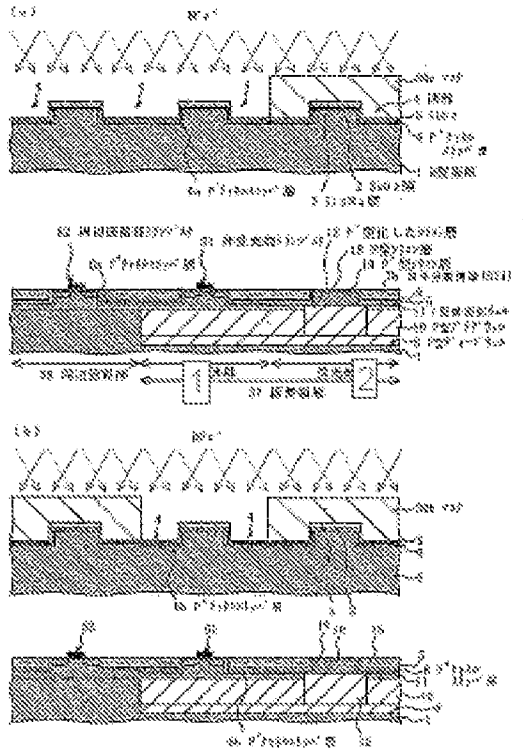
(i) Process 9: B^+ injected to below STI structure to form p-type surface-side well
1) Non-light-receiving section
2) Light-receiving section

(j) Process 10: As^+ injected in sensor opening section

(k) Process 11: $BF2^+$ injected into light-receiving region

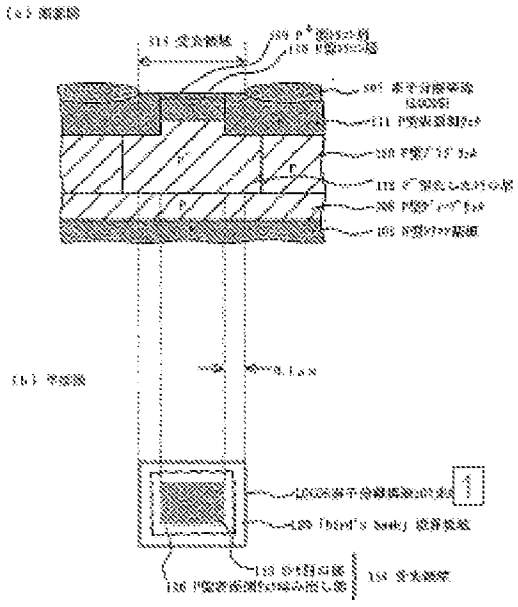
(l) Process 12: Semiconductor circuit element formed

[Figure 8] Another example of CMOS image sensor



Key:
1) Non-light-receiving section
2) Light-receiving section

[Figure 9] PD section of conventional image sensor



(a) Cross sectional view

(b) Top view

1) End of LOCOS element-isolating structure 107